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EXAMINER	
VOCKRODT, JEFF B	
ART UNIT	**PAPER NUMBER**
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/854,177	Applicant(s) XU ET AL.	
	Examin r Jeff Vockrodt	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47,55 and 65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36,40-47,55 and 65* is/are rejected.

7)☒ Claim(s) *37-39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5,7 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the election filed May 15, 2003. Claims 1-47, 55, and 65 are pending. The cancellation of all non-elected claims in response to the restriction requirement mailed May 6, 2003 is noted.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5, 8-29, and 41-47 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pat. No. 6,011,404 ("Ma").

Ma teaches improved corona oxide semiconductor (COS) processes that permit measurement of tunneling characteristics in addition to conventional mobile charge contamination determination that was afforded by conventional COS (col. 2, ll. 34-46; col. 3, ll. 5-15). Ma teaches COS techniques for measuring mobile charge in the oxide due to metal contamination (col. 6, ll. 37-43) that are similar to those disclosed by Edelman and include: corona charge, heat cycles for temperature stress measurements, and surface voltage drop measurements. In addition to measuring mobile charge, tunneling field is measured using the non-contact COS techniques to complete the established metrics for dielectrics (col. 2, ll. 34-46 and col. 11, ll. 33-36).

The overall process of Ma comprises:

(1) depositing charge on an oxide layer (initial corona charging step);

(2) thermally stressing the oxide to redistribute mobile charges that are under the influence of the deposited charge within the oxide;

(3) measuring the surface voltage change;

(4) obtaining the mobile charge from the measured change in surface voltage to determine the amount of metal contamination (surface voltage drop that is directly proportional to the amount of mobile charge during heating cycle causes mobile charge to be "pushed or pulled" across the oxide; col. 6, ll. 37-43);

(5) measuring the tunnel voltage of the oxide (¶ bridging cols. 3-4; col. 11, ll. 1-56; claim 21); and

(6) determining the total oxide charge fluence, which is a function of bulk oxide impurities ("[iron] severely affects oxide integrity by lowering breakdown voltage as a function of iron concentration" col. 7, ll. 5-6; "Bulk oxide impurities can lower E_{tun} by introducing hopping conduction paths in the oxide" col. 10, ll. 63-65; and "[t]unneling field plots can be analyzed to determine the total oxide charge fluence (i.e., the amount of charge that actually flows through the oxide during the E_{tun} test)," col. 11, ll. 38-40).

Claim 1 reads on Ma as follows: A method for detecting metal contamination in a dielectric material disposed upon a semiconductor substrate, comprising: annealing[1] the semiconductor substrate, wherein annealing the semiconductor substrate is effective to drive the metal contamination into the dielectric material (step 2); measuring a

[1] The term "annealing" is read broadly to cover the heating and cooling used to redistribute contaminants for stress measurement. "[D]uring examination proceedings, claims are given their broadest reasonable interpretation consistent with the specification." In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000) (citing In re Graves, 69 F.3d 1147,1152, 36 USPQ2d 1697,1701 (Fed. Cir. 1995); In re Etter, 756 F.2d 852, 858, 225 USPQ 1, 5 (Fed. Cir. 1985) (en banc)). Claim 6, which depends from claim 1, distinguishes over Ma in this aspect by requiring "an annealing temperature of approximately 350 °C to approximately 500 °C."

tunneling voltage of the dielectric material (step 5); and determining a characteristic of the metal contamination in the dielectric material, wherein the characteristic is a function of the measured tunneling voltage (step 6).

Claim 2. The method of claim 1, wherein the annealed dielectric material is substantially free of damage (Ma is a non-contact process with a low temperature anneal--200 to 250°C).

Claim 3. The method of claim 1, wherein annealing the semiconductor substrate comprises heating the semiconductor substrate to an annealing temperature, and wherein the metal contamination comprises one type of metal contamination (the heating occurs after charge is deposited; iron is one type of metal contamination; see treatment of claim 1).

Claim 5. The method of claim 1, wherein annealing the semiconductor substrate comprises heating the semiconductor substrate to an annealing temperature of less than approximately 1100 °C (the annealing temperature is 200-250°C; col. 6, ll. 37-43).

Claim 8. The method of claim 1, wherein measuring the tunneling voltage comprises depositing a charge on an upper surface of the dielectric material, and wherein depositing the charge comprises using a non-contact corona charging technique (col. 8, ll. 4-6).

Claim 9. The method of claim 1, wherein measuring the tunneling voltage comprises depositing a charge on an upper surface of the dielectric material, and wherein the deposited charge comprises approximately 1x10-6 C/cm2 to approximately 1x10-4 C/cm2 for positive tunneling voltage ("9E-6 C/cm^{2}"; col. 11, ll. 1-5).

Claim 10. The method of claim 1, wherein measuring the tunneling voltage comprises depositing a charge on an upper surface of the dielectric material, and

wherein the deposited charge comprises approximately -1x10-6 C/cm2 to approximately -1x10-4 C/cm2 for negative tunneling voltage (see treatment of claims 8 and 9).

Claim 11. The method of claim 1, wherein measuring the tunneling voltage comprises: depositing a charge on an upper surface of the dielectric material; waiting for a predetermined period of time after depositing a charge on an upper surface of the dielectric material; and determining the tunneling voltage (the heating step necessarily takes time; see treatment of claim 1).

Claim 12. The method of claim 1, wherein measuring the tunneling voltage comprises depositing a charge on an upper surface of the dielectric material, and wherein depositing a charge on an upper surface of the dielectric material comprises depositing the charge on predetermined regions of the upper surface of the dielectric material (Fig. 3A).

Claim 13. The method of claim 1, wherein measuring the tunneling voltage comprises depositing a charge on an upper surface of the dielectric material, and wherein depositing the charge on the upper surface of the dielectric material comprises depositing the charge on a portion of the upper surface or on substantially the entire upper surface (Fig. 3A).

Claim 14. The method of claim 1, wherein measuring the tunneling voltage of the dielectric material comprises using a non-contact work function measurement technique (see treatment of claim 1; Ma is clearly non-contact and measuring voltage changes as mobile ions are "pushed or pulled" is clearly a work function method).

Claims 15-19, 21, 25-29, and 45-46. Ma teaches making tunneling field plots which involve multiple measurements of tunneling voltage (col. 11, ll. 23-55).

Claim 20. The method of claim 1, further comprising determining a tunneling field of the dielectric material, wherein the tunneling field is a function of the tunneling voltage (col. 11, ll. 1-36).

Claim 22. The method of claim 1, wherein the characteristic of the metal contamination further comprises a function of a temperature of the annealing of the semiconductor substrate. (This property is inherent in Ma; the claim does not require anything more than the property be present.)

~~Claim 23. The method of claim 1, wherein the characteristic of the metal~~ contamination further comprises a function of an amount of the deposited charge. (col. 11, ll. 6-22)

Claim 24. The method of claim 1, wherein determining the characteristic of the metal contamination in the dielectric material comprises determining a characteristic of at least two types of metal contamination in the dielectric material (see treatment of claim 4).

Claim 41. The method of claim 1, wherein the dielectric (12; Fig. 1) material comprises silicon dioxide, silicon nitride, or silicon oxynitride.

Claim 42. The method of claim 1, wherein the semiconductor substrate (10, Fig. 1) comprises monocrystalline silicon, silicon germanium, or gallium arsenide.

Claim 43. The method of claim 1, wherein the metal contamination comprises copper (col. 7, ll. 49-57).

Claim 44. The method of claim 1, wherein the metal contamination comprises iron, chromium, cobalt, or aluminum (col. 7, ll. 49-57).

Claim 47 reads on Ma as follows: A method for increasing degradation of a dielectric material resulting from metal contamination, comprising: generating electrical stress in the dielectric material, wherein the dielectric material is disposed upon a

semiconductor substrate (depositing a corona charge); and heating the semiconductor substrate subsequent to generating electrical stress in the dielectric material (thermal cycles associated with metal contamination detection).

Claims 47 and 65 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. No. 5,773,989 ("Edelman").

Edelman teaches measurement of the mobile sodium ion concentration in a silicon oxide layer on a silicon wafer comprising the following sequential steps:

(1) depositing a negative charge on the oxide layer using corona discharge (Figs. 5A-5B; and step 202, Fig. 7);

(2) performing a temperature stress step to mobilize sodium ions in the oxide layer freeing them to repel from the deposited charge (Fig. 5B; step 206, Fig. 7);

(3) measuring the contact potential distribution to determine to contact potential shifts (steps 210, 212, Fig. 7); and

(4) determining the mobile ion concentration from the shift in contact potential (step 214, Fig. 7).

Claim 47 reads on Edelman as follows: A method for increasing degradation of a dielectric material resulting from metal contamination, comprising: generating electrical stress in the dielectric material, wherein the dielectric material is disposed upon a semiconductor substrate (step 1 above); and heating the semiconductor substrate subsequent to generating electrical stress in the dielectric material (step 2 above).

Claim 65 reads on Edelman as follows: A method for detecting metal (sodium) contamination in a dielectric material disposed upon a semiconductor substrate, comprising: annealing the semiconductor substrate, wherein annealing the semiconductor substrate is effective to drive the metal contamination into the dielectric material (step 2 above); measuring an electrical property of the dielectric material (step 3

above); and determining a characteristic of the metal contamination in the dielectric material, wherein the characteristic is a function of the measured electrical property (step 4 above).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8-35, 41-47, and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,569,691 ("Jastrzebski") in view of Ma.

Jastrzebski teaches a noncontact technique for measuring multiple ion concentrations in a silicon dioxide layer. Specifically, Jastrzebski deals with the problem of copper deposited on the oxide surface and penetrating into the silicon oxide layer during annealing at temperatures of between 400-500°C in the presence of alkaline impurities (col. 1, ll. 9-29). An advantage of Jastrzebski is that different mobile ion concentrations can be measured (col. 2, ll. 35-36). Figs. 8A-8F show a sequence in which two different metal ion concentrations are measured using a noncontact methodology.

Claim 1 corresponds to Jastrzebski as follows (underlining omissions): A method for detecting metal contamination in a dielectric material disposed upon a semiconductor substrate, comprising: annealing the semiconductor substrate, wherein annealing the semiconductor substrate is effective to drive the metal contamination into the dielectric material (400-500°C anneals that give rise to copper contamination problem); [Jastrzebski uses a noncontact method to determine the mobile ion

concentrations; Fig. 8A-8F][2]; measuring a tunneling voltage of the dielectric material; and determining a characteristic of the metal contamination in the dielectric material, wherein the characteristic is a function of the measured tunneling voltage.

Jastrzebski measures only mobile ion concentration of the copper and alkali ions in the oxide layer, and does not teach measuring the tunneling voltage as required by the claims.

Ma is discussed above. Ma generally teaches that measuring tunneling voltage in addition to conventional mobile charge contamination (mobile ion concentration) is advantageous to complete the established metrics (including charge fluence determination) for dielectrics using a single COS system. (Ma, col. 11, ll. 37-41).

Jastrzebski and Ma are within the same field of endeavor--non-contact measurement processes for characterizing semiconductor wafers.

It would have been obvious to one of ordinary skill in the art at the time of the invention to measure the tunneling voltage of the dielectric material and use it to determine the charge fluence in the process of Jastrzebski. One of ordinary skill in the art would have been motivated to do this to complete the established metrics for dielectrics using a single COS system as taught by Ma.

Claims 1-3, 5, 8-29, and 41-47 are met by Ma as discussed above. These claims also read on the subject matter of Jastrzebski in view of Ma, except here, the step 1 of annealing taught by Jastrzebski reads on "annealing the semiconductor substrate" whereas the subsequent steps are taught by Ma as discussed above.

[2] This mobile ion concentration determination step is not required by the claims, although it is permitted by them, and is only inserted to underscore what is taught by Jastrzebiski.

Claim 4. The method of claim 1, wherein the metal contamination comprises at least two types of metal contamination (Jastrzebski teaches copper and alkali contamination as discussed above).

Claim 6. The method of claim 1, wherein the metal contamination comprises copper, and wherein annealing the semiconductor substrate comprises heating the semiconductor substrate to an annealing temperature of approximately 350 °C to approximately 500 °C (Jastrzebski, col. 1, ll. 9-29)

Claim 22. The method of claim 1, wherein the characteristic of the metal contamination further comprises a function of a temperature of the annealing of the semiconductor substrate. (This property is inherent in Jastrzebski; the claim does not require anything more than the property be present.)

Claim 30. The method of claim 1, further comprising annealing the semiconductor substrate subsequent to depositing the charge on an upper surface of the semiconductor substrate. (Jastrzebski, Figs. 8A-8f).

Claim 31-32 and 35. The method of claim 30, further comprising heating the semiconductor substrate to an annealing temperature of less than approximately 120 °C. Jastrzebski teaches 150°C which is approximately 120°C. The specification moreover does not prove the criticality of this range. Both temperatures are used as temperature stress bias temperatures and the time and specific ion as well as temperature affects ion mobility. One of ordinary skill in the art would have appreciated that lowering the temperature would increase the amount of time particular ions take to transport across the oxide and would have been motivated to decrease the temperature where necessary to achieve a desired separation in the process of Jastrzebski.

Claim 33. The method of claim 1, further comprising generating electrical stress in the dielectric material and heating the semiconductor substrate subsequent to generating the electrical stress in the dielectric material (Jastrzebski, Figs. 8A-8f).

Claim 34. The method of claim 33, wherein generating electrical stress comprises using a non-contact corona charging technique, and wherein the electrical stress comprises approximately -1 x 10-3 C/cm2 to approximately +1 x 10-3 C/cm2. (Ma teaches a charge of 0.74E-8 C/cm2 (Ma, col. 5, ll. 15), which is within the claimed range.)

Claim 55. A method for determining a characteristic of metal contamination in a dielectric material disposed upon a semiconductor substrate, comprising: annealing the semiconductor substrate prior to depositing a charge on an upper surface of the dielectric material, wherein annealing the semiconductor substrate is effective to drive the metal contamination into the dielectric material (Jastrzebiski; copper contamination from annealing); depositing a charge upon the upper surface of the dielectric material (Jastrzebiski; Figs. 8A-8F); annealing the semiconductor substrate subsequent to depositing a charge on the upper surface of the dielectric material (Jastrzebiski; Figs. 8A-8F); measuring a tunneling voltage of the dielectric material (Ma; measuring tunneling voltage); and determining a characteristic of the metal contamination in the dielectric material, wherein the characteristic is a function of the measured tunneling voltage (Ma; determining charge fluence).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ma in view of Edelman.

Ma is discussed above. Ma teaches a heating or annealing step (step 2: thermally stressing), but does not teach "wherein annealing the semiconductor substrate

comprises heating the semiconductor substrate for a period of time, and wherein the period of time comprises approximately one minute to approximately thirty minutes."

Edelman teaches a COS process for measuring mobile ion concentration in an oxide layer wherein a thermal stressing step is carried out for 4 minutes; col. 6, ll. 56-59.

It would have been obvious to one of ordinary skill in the art at the time of the invention to carry out the thermally stressing step for 4 minutes in the process of Ma. One of ordinary skill in the art would have been motivated to use a conventional thermal stressing duration taught by Edelman since Ma does not teach a time period for this step and Ma and Edelman are similar processes.

Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jastrzebiski in view of Ma as applied to claim 33 above, further in view of Edelman.

Claim 36. The method of claim 33, wherein heating the semiconductor substrate comprises heating the semiconductor substrate for a period of time of approximately one minute to approximately thirty minutes. The reasons for rejecting claim 36 are analogous to that in the rejection of claim 7 under 35 U.S.C. 103(a) as being unpatentable over Ma in view of Edelman set forth above.

Allowable Subject Matter

Claims 37-39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 37 and 38-39, which depend from claim 37:

Claim 37. The method of claim 1, further comprising determining a presence of particulate contamination on the dielectric layer, wherein the presence of particulate contamination is a function of the measured tunneling voltage. None of the references

of record teach or motivate applying the processes in Jastrzebski, Ma, or Edelman to determining a presence of particulate contamination on the dielectric layer

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cosway et al., Manufacturing Implementation of Corona Oxide Silicon (COS) Systems for Diffusion Furnace Contamination Monitoring, 1997 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop ASMC 97 Proceedings, Cambridge, MA, USA, 10-12 Sept. 1997, pp. 98-102. Cosway uses noncontact techniques similar to those of Jastrzebski, Ma, and Edelman to determine iron contamination after an annealing process.

Any inquiry concerning communications from the examiner should be directed to Jeff Vockrodt at (703) 306-9144 who can be reached on weekdays from 9:30 am to 5:00 pm EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached at (703) 308-4905.

The fax numbers for this Group are (703) 305-3432, (703) 308-7722, (703) 305-3431, and (703) 308-7724. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist at (703) 308-0956.

May 30, 2003
J. Vockrodt

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